CLAIMS

1. A vertical power transistor trench-gate semiconductor device (100) having a trench network (STR1, ITR1) extending into a semiconductor body (10) and surrounding a plurality of closed transistor cells (TCS), wherein the trench network comprises segment trench regions (STR1) adjacent sides of the transistor cells (TCS) and intersection trench regions (ITR1) adjacent corners of the transistor cells, wherein each transistor cell (TCS) has a source region (24) and a drain region (12) which are vertically separated by a channel-accommodating body region (23) adjacent a segment trench region (STR1) at each side of the transistor cell, and wherein each segment trench region contains gate material (22) separated from the semiconductor body (10) by insulating material (21) at the vertical sides and at the bottom of the segment trench region (STR1), wherein the intersection trench regions (ITR1) each include insulating material (21C, 21D) which extends from the bottom of the intersection trench region with a thickness which is greater than the thickness of the insulating material (21B1) at the bottom of the segment trench regions (STR1), gate material (22) being provided above the insulating material (21C, 21D)in the intersection trench regions (ITR1) and bridging the gate material (22) in the segment trench regions (STR1), wherein the greater thickness of the insulating material (21C, 21D) extending from the bottom of the intersection trench regions (ITR1) is effective to increase the drain-source reverse breakdown voltage of the device (100).

2. A device as claimed in claim 1, wherein the insulating material (21B1′) is thicker at the bottom of the trench segment regions (STR1) than at the vertical sides (21A1) of the trench segment regions so as to reduce the gate-drain capacitance of the device (100), and wherein the greater thickness of insulating material (21C′) extending from the bottom of the intersection trench regions (ITR1) further reduces the gate-drain capacitance of the device.

3. A device as claimed in claim 1 or claim 2, wherein the closed transistor cells (TCS) are each rectangular shaped with a said segment trench region (STR1) adjacent each one of four sides of the cell.

4. A device as claimed in claim 3, wherein the closed transistor cells (TCS) are square shaped.

5. A device as claimed in claim 3 or claim 4, wherein each intersection trench region (ITR1) has a square shaped area.

6. A device as claimed in claim 3 or claim 4, wherein each intersection region (ITR5) has a cruciform shaped area.

7. A device as claimed in claim 1 or claim 2, wherein the closed transistor cells (TCH) are each hexagonal shaped with a said segment trench region (STR2) adjacent each one of six sides of the cell (TCH).

8. A device as claimed in any preceding claim, wherein at least that part of the insulating material (21C) which extends from the bottom of each intersection trench region (ITR1) nearest the corners of the adjacent transistor cells (TCS) extends upwards (21A4) to thicken the insulating material at least at these corners over at least part of the vertical extent of the channel-accommodating body region (23) so as to increase the threshold voltage of the device.

9. A device as claimed in claim 8, wherein the insulating material (21C) in each intersection trench region (ITR1) which is thickened over at least part of the vertical extent of the channel-accommodating region (23) is so thickened (21A4) only at a peripheral part of the area of intersection trench region (ITR1).

10. A device as claimed in claim 8, wherein the insulating material (21D) which extends from the bottom of each intersection trench region (ITR1) has the same thickness over the whole area of the intersection trench region.

11. A device as claimed in any preceding claim, wherein the semiconductor body (10) is silicon and wherein the insulating material at the bottom (21B1) of the segment trench regions (STR1) and the insulating material extending from the bottom (21C, 21D) of the intersection trench regions (ITR1) is silicon dioxide.

12. A method of making a device as claimed in any preceding claim, the method including

a first sequence of steps (Figures 20-25, 30) at the conclusion of which there are provided trenches for the intersection trench regions (ITR1) with the insulating material (32, 32B) which extends from the bottom of the intersection trench regions, and in which there are provided empty trenches (TR1, TR2) for the segment trench regions (STR1), and

a second sequence of steps (Figure 26) at the conclusion of which there is provided the insulating material at the vertical sides (21A1) and bottom (21B1) of the segment trench regions (STR1), and also there is provided the gate material (22) in the segment trench regions and above the insulating material (32) in the intersection trench regions.

13. A method as claimed in claim 12, wherein the first sequence of steps includes

etching a first set of parallel trenches (TR1) in areas to be occupied by some of the segment trench regions (STR1) and in areas to be occupied by the intersection trench regions (ITR1),

providing the insulating material (32) which will extend from bottom of the intersection trench regions in the final device within and along the whole length of the first set of trenches (TR1),

etching a second set of trenches (TR2) in areas to be occupied by the remainder of the segment trench regions (STR1),

providing a different insulating material (33) to fill the second set of trenches (TR2) and to cover the insulating material (32) in the intersection trench regions (ITR1),

removing the insulating material (32) from the segment trench regions (STR1) of the first set of trenches (TR1), and then removing the different insulating material (33).